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(71) Applicant(s)
Circuit Components Incorporated

(Incorporated in USA - Arizona)

2400 South Roosevelt Street, Tempe 85282, Arizona, United States of America

(72) Inventor(s)
Norman L Greenman
M. P. Ramachandra Panicker
Jorge M Hernandez

(74) Agent and/or Address for Service
Marks & Clerk
Alpha Tower, Suffolk Street Queensway, BIRMINGHAM, B1 1TT, United Kingdom

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(58) Field of Search
UK CL (Edition O) H1K KRG KRLX KRX
INT CL^6 H01L 21/48 23/498 23/50 , H05K 3/34
Online:WPI

(54) IC package with a ball grid array on a single layer ceramic substrate

(57) A Digital Integrated Circuit Package is disclosed which exhibits a large input/output (10) capability while maintaining a small footprint. The package employs a Ball Grid Array (BGA) format and a single layer ceramic substrate with bimetallic filled precisely positioned vias 22, 25. Some of the vias 25 are located for heat conduction from a die 30. The conductive balls 17 of the array may be of copper or lead/tin solder. A protective layer 31 is provided outside a cover 32. In other arrangements the die is encapsulated in epoxy material, and the die may be flip-mounted with the cover extending to the edge of the substrate.

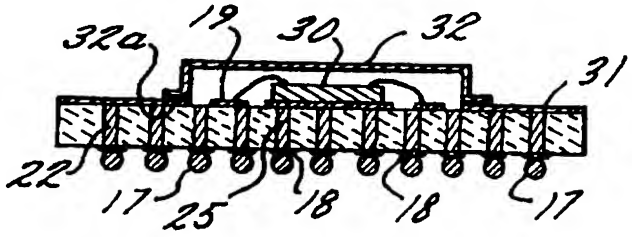

FIG. 5

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At least one drawing originally filed was informal and the print reproduced here is taken from a later filed formal copy.

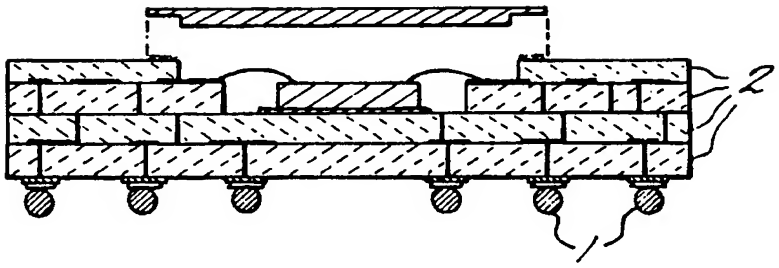

FIG. 1
(PRIOR ART)

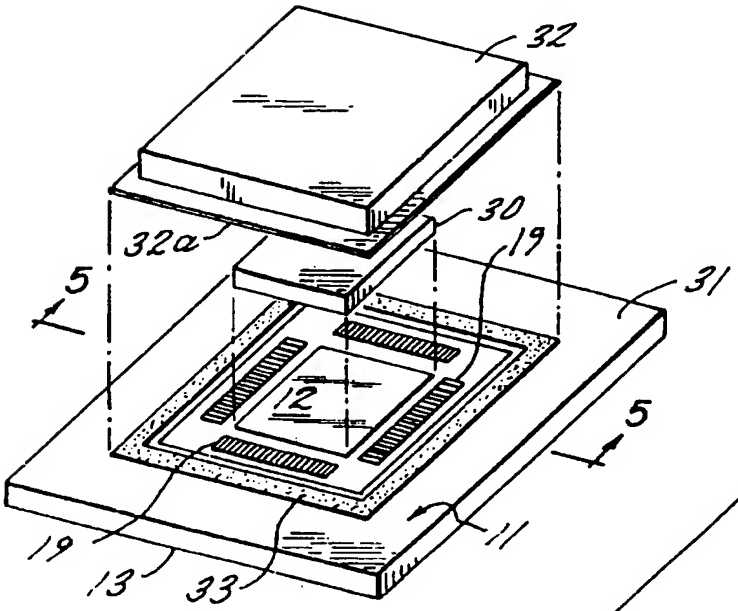

FIG. 2

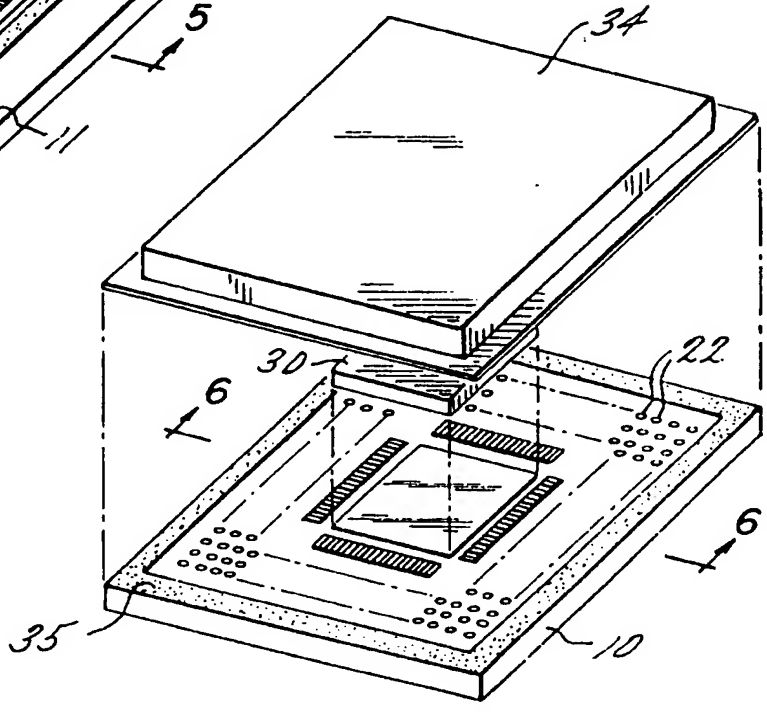

FIG. 3

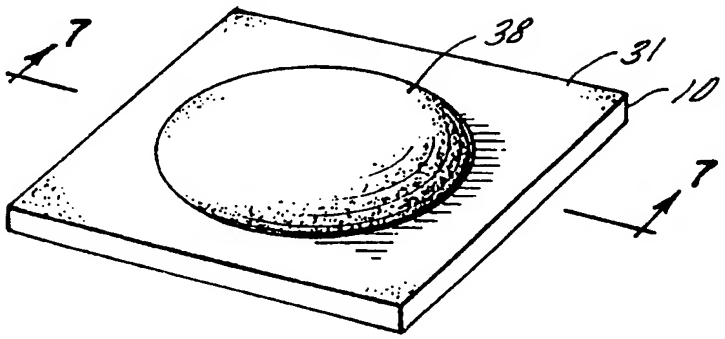

FIG. 4

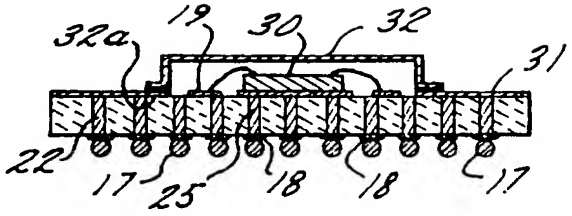

FIG. 5

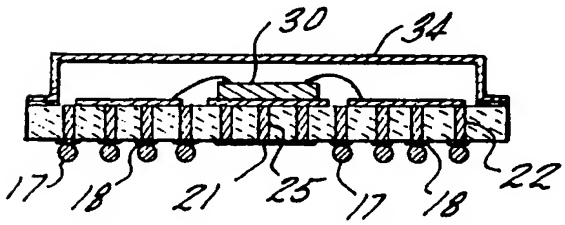

FIG. 6

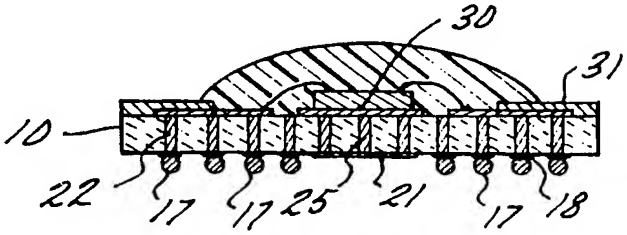

FIG. 7

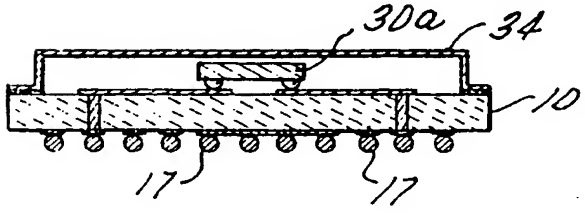

FIG. 8

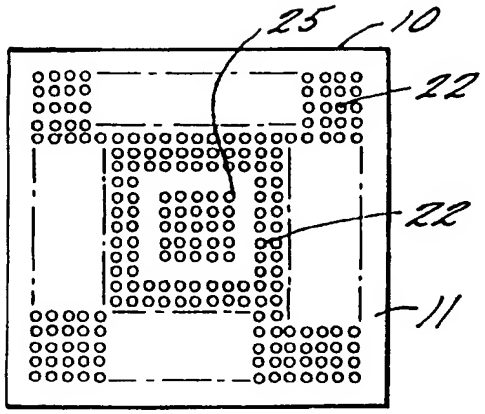

FIG. 9

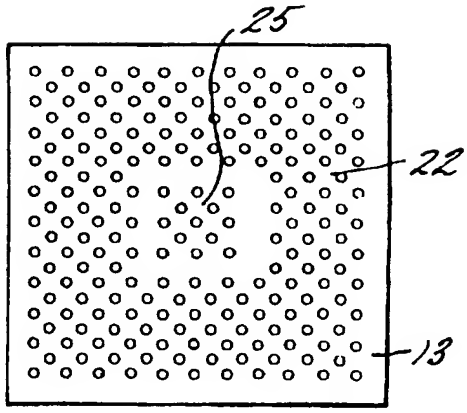

FIG. 10

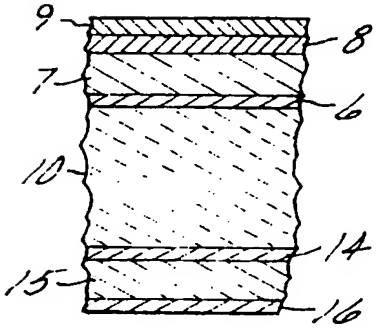

FIG. 11

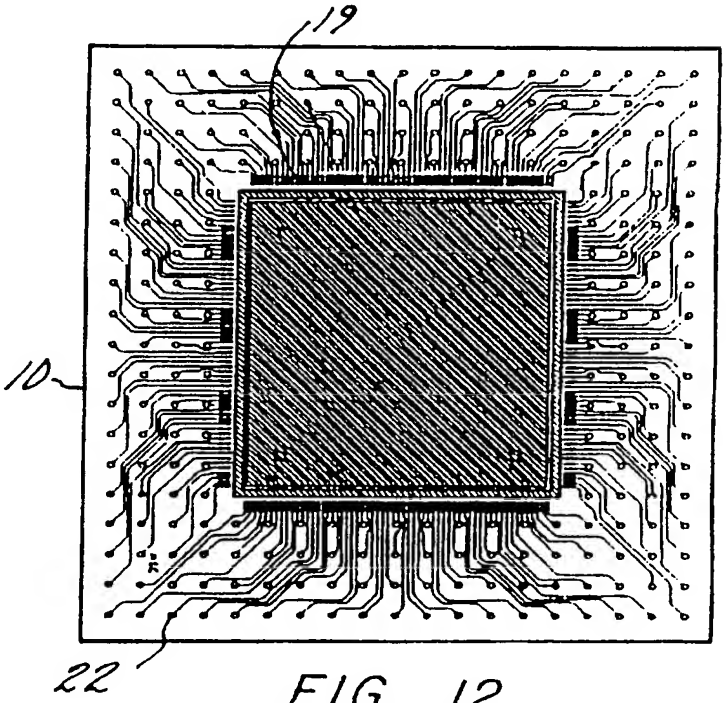

FIG. 12

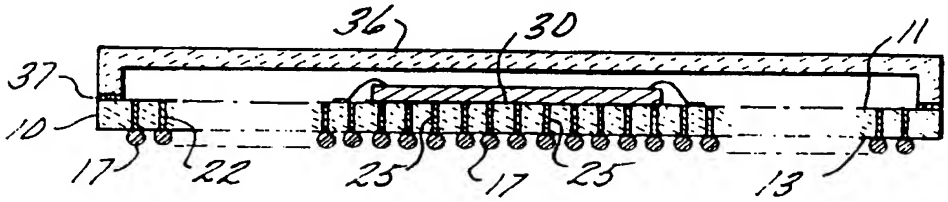

FIG. 13

A HIGH PERFORMANCE DIGITAL IC PACKAGE, USING BGA (BALL GRID ARRAY) I/O FORMAT, AND SINGLE LAYER CERAMIC SUBSTRATE WITH BIMETALLIC FILLED VIA TECHNOLOGY

Cross-Reference to Related Application:

This is a continuation-in-part of U.S. Patent Application Serial No. 08/398,586 filed March 2, 1995.

Background of the Invention:

Field of the Invention

This invention relates to the field of single and multiple chip packages for digital integrated circuits. More particularly, this invention relates to a single layer ceramic substrate supporting a multiplicity of bi-metallic or tri-metallic vias connected to a Ball Grid array, to promote a larger number of connections in a small unit area.

One of todays' successful package styles for single and multiple IC chips, uses the BGA (Ball Grid Array) I/O format, as opposed to LGA (Land Grid Array), or leaded package styles. This is so because the BGA format is conducive to higher I/O content than a practical leaded package of the same size and it can be easily installed on a PC Board, especially when solder balls are used for the BGA. This is in contrast to an LGA package, which has the same I/O density, but requires socketing because otherwise assuring the quality of solder joints when the package is mounted flush over the PCB, is extremely difficult, if not impossible.

Among the presently known BGA packages, there are a number of construction schemes with advantages and disadvantages, as follows:

BGA packages using ceramic construction employ a multilayer cofired structure. A multilayer structure is needed because the shrinkage inherent to the process, in addition to the drawbacks of thick film screen printable refractory metal conductive pastes, limit the physical size (line width and spacing, via capture pad diameters, etc.) of interconnection circuitry required to bring in signals from the PC Board to the IC chip(s) and vice versa. A single ceramic layer lacks sufficient surface area to accommodate the number of traces and pads needed to completely connect the desired IC's. To alleviate the situation, prior art constructions employed multiple layer construction. Drawbacks

are experienced with this method in that as the number of I/O's grows, so does the number of layers, if the package size is to be maintained as small as possible.

An increased number of layers (and package size) aggravates the problem of electrical parasitics which adversely affect the performance of the semiconductor device.

Also, the increased number of layers bring about alignment and registration problems between layers, which are aggravated by the shrinkage of the structure during sintering. Yields of these packages are adversely affected thereby, and costs associated with production of the packages is increased. Generally speaking, multilayer cofired ceramic packages are more expensive than other alternatives.

Another type of construction employing glass and ceramic material alleviates to a significant extent, the problem created by shrinkage, since the glass-ceramic material is designed to minimize shrinkage. However, since the circuitry is still screen printed, and screen printing is a process with limited resolution capability, there is a limit to the number of traces and pads that can be accommodated on a single layer. Therefore, there is still the need for a multilayer structure like that above. As will be appreciated, this translates to higher cost than other alternatives.

In yet another prior art configuration, an epoxy-fiberglass board is patterned on one side to receive the array of solder balls, whereas the opposite surface (or layers) are circuit patterned using plated through holes for interconnection between layers. Improved photoresist-etching technology is employed to achieve line widths/spacings in the vicinity of 0.003"- 0.004" (75 to 100 micrometers). This is known as Plastic Ball Grid Array construction. There are two significant problems with this type of construction: (1) is that as the number of I/O's increases, the cost of the package becomes prohibitive, especially if the package size is to be kept to a minimum; (2) is that as the I/O count increases, so (in general) does the power dissipated by the IC chip. Because of an inability of the package to dissipate the heat generated by the IC chip in an adequate manner these chips are prone to early failure. For this reason, common commercial

devices such as Intel's Pentium Processors which are configured with PGA ceramic packages must employ fans mounted directly on top of the package to remove heat therefrom.

A major problem with ceramic multilayer, glass ceramic and plastic ball grid array constructions is the difficulty in achieving the flatness on the two large surfaces of the package, needed for coplanarity of the ball array or for flip chip mounting of the semiconductor device. Cofired multilayer ceramic structures and PCB laminates have inherent camber problems.

Another problem with multilayer cofired ceramic BGA packages is the poor coplanarity of the balls once they are attached to the package, making difficult the assembly of the packaged IC. The nominal coplanarity of multilayer ceramic BGA packages is only 0.006", which is considered excessive in the industry. In the package of the present invention, the coplanarity can be tightly controlled.

The package of the present invention alleviates or significantly reduces the problems and limitations of BGA packages of the prior art.

Other prior art includes U.S. Pat. 5,089,881 to Panicker, U.S. Pat. 4,942,216 to Panicker (both of which are fully incorporated herein by reference) and other pin grid array configurations. An exemplary multilayer BGA package is illustrated in FIGURE 1.

Moreover, Amkor produces a plastic BGA package which uses PCB technology to create circuit traces and side-to-side connections.

Summary of the Invention:

The above-discussed and other drawbacks and deficiencies of the prior art are overcome or alleviated by the Ball Grid Array IC package of the invention.

The present invention employs a fully sintered ceramic, single layer substrate or other material having similar characteristics. Vias are subsequently laser drilled in

a multiplicity of places in a generally regular pattern and with both thermal vias and signal/power vias being provided for. Vias are filled with a bi-metallic or tri-metallic composite material. The whole substrate is then metalized by a number of alternative methods and metals including thin film titanium, chromium, molybdenum, tungsten or a combination thereof, copper and nickel. Pads may also be of the copper thick film variety. The balls for the BGA will generally be of a lead/tin alloy and be brazed onto the ball side of substrate.

In order to more effectively dissipate heat from the thermal vias a heat spreader pad is metalized over the thermal vias in several methods as outlined above. Pads are also provided around the heat spreader for connection to the wirebonds or flip-chip. These pads are connected to the appropriate vias by traces approximately 0.002 inch wide width spacings therebetween of 0.002 inch.

The metalization of the die attach side of the substrate is as follows: 1) Adhesion promoter bonded to substrate; 2) current carrying material bonded to adhesion promoter; 3) buffer material bonded to current carrying material; 4) protective finish bonded to buffer.

Completing the package is accomplished in one of three preferred ways including arranging a metallic or metal plated lid over the die and bonding pads but leaving the protective coating exposed; arranging a similar lid or ceramic lid to cover the entire substrate, or applying a "blob" of epoxy over the die and wirebonds.

The invention provides a mimimally dimensioned package which avoids the drawbacks of multiple layering while maintaining a low cost.

The above-discussed and other features and advantages of the present invention will be appreciated and understood by those skilled in the art from the following detailed description and drawings.

Brief Description of the Drawings:

Referring now to the drawings wherein like elements are numbered alike in the several FIGURES:

FIGURE 1 is a cross section view of a prior art multilayer substrate and a ball grid array;

FIGURE 2 is a perspective exploded view of one embodiment of the invention;

FIGURE 3 is a perspective exploded view of a second embodiment of the invention;

FIGURE 4 is a perspective exploded view of a third embodiment of the invention;

FIGURE 5 is a sectional view taken along section lines 5-5 in FIGURE 2;

FIGURE 6 is a sectional view taken along lines 6-6 in FIGURE 3;

FIGURE 7 is a sectional view taken along lines 7-7 in FIGURE 4;

FIGURE 8 is an exemplary sectional view of an embodiment employing a flip-chip;

FIGURE 9 is a plan view of a substrate with drilled vias where the vias are in a regular pattern;

FIGURE 10 is a plan view of a substrate with drill vias where the vias are in an interstitial pattern;

FIGURE 11 is a schematic view of a substrate of the invention illustrating the layers of metalization on both the die attach side and BGA side;

FIGURE 12 is a plan view of the die attach side of the substrate illustrating the trace pattern of the package;

FIGURE 13 is a cross section of a package with a size matched ceramic cover.

Detailed Description Of The Preferred Embodiments:

Referring to FIGURE 1 a prior art multiple layer Ball Grid Array (BGA) is illustrated in cross section. As will be recognized by one of skill in the art, in order to

achieve a sufficient number of balls 1 for the array, multiple layers 2 of substrate are necessary all of which contribute to the drawbacks discussed in the Background of the Invention set forth above. It is these drawbacks, *inter alia*, which the present invention solves by maintaining a single layer substrate while providing a larger number of interconnection sites in the form of balls in a Ball Grid Array (BGA).

It should be noted that the basic concept of the invention is similar throughout the following description and that preferred embodiments are merely modifications of the concept. For the ensuing discussion, each of the drawings may be generally referred to.

In the most general description, the invention employs a single layer substrate 10 comprising a fully sintered ceramic material. Preferred materials include but are not limited to Aluminum oxide (Al_2O_3), Aluminum Nitride (AlN), Beryllium Oxide (BeO), Boron Nitride (BN), Silicon Carbide (SiC), etc. Known sintering methods are utilized to form this substrate material. Preferred starting thickness of the substrate 10 for use in the invention is approximately 0.040 inch.

Once the substrate 10 is fully prepared, vias 22 and 25 are drilled in a predetermined pattern. It will be appreciated that vias 22, 25 may be drilled by any suitable method, however it is preferred to employ a computer controlled laser to very precisely locate the vias in the predetermined position.

It is preferred to place a large number of thermal vias 25 in a central location on the substrate 10, which location will correspond with the location of the die 30 to be placed thereon. The thermal vias 25 thus draw heat from the die 30 and cooperate with structures to be discussed hereunder to dissipate the collected heat. Power and signal vias 22 are located along the periphery of the substrate 10. Alternately, power and ground vias can be placed under the chip, especially when the application is for flip chip die attachment. All vias are generally spaced from each other in columns or rows by about 0.050 inch. In a regular pitch, as illustrated in FIGURE 9, the above is the only dimension between vias. Where an interstitial pitch is employed, however, it will be

recognized from FIGURE 10 that rows and columns are still spaced therealong at about 0.050 inch between vias but since the rows are staggered, the distance between each columnar via in adjacent rows are merely about 0.025 inch apart. This provides for a larger number of vias in a unit area without losing the 0.050 inch clearance between vias in each column or row. Both are fully functional. In flip chip assembly applications, smaller and irregular via patterns are often employed to accommodate the pad layout of the IC die.

Vias 22, 25 are filled with preferably a bi-metallic or tri-metallic composite such as with W-Cu or with W-CuAg (wherein the CuAg is an eutectic CuAg alloy). Vias may be filled with these materials in ways known per se.

Subsequently to via filling the final thickness of the substrate is achieved by lapping to both the die attach surface 11 and the ball attach surface 13 and finishing to less than about 2.0 microinch Ra.

Referring to FIGURE 11, one will appreciate the metalization of the surfaces of substrate 10. Die attach surface 11 is depicted on the upper side of substrate 10 in the FIGURE whereas Ball attach surface 13 is depicted on the lower surface of substrate 10 in the FIGURE.

Die attach surface 11 includes adhesion promoter 6 bonded directly to the ceramic substrate 10. Promoter 6 most preferably comprises thin film Chromium, thin film Titanium or thin film Titanium/Tungsten, Titanium/Molybdenum in a thickness of approximately 500-2000Å, however the promoter may be any material which provides sufficient adhesion to both the ceramic material employed for the substrate and to a current carrier layer 7 which is bonded to the promoter 6. Current carrier 7 most preferably is comprised of copper in a thickness of approximately 5-10 micrometers because of its excellent electrical/conductive properties. Following carrier 7, a buffer 8 is deposited, buffer 8 is commonly nickel in a thin film form of about 1 about 3.5 micrometers in thickness. The buffer is to prevent diffusion of Copper into the final

protective finish. Finally, protective finish 9 is added, gold being the preferred material, in a thickness of about 2 about 3.5 micrometers. It should be noted that all metalization layers deposited on die attach surface 11 as well as on Ball attach surface 13 may be applied by any conventional deposition method including but not limited to: sputtering, enhanced ion plating, low temperature Arc Vapor deposition.

Where a flip chip is employed it is sometimes desirable to alternatively metalize as follows: promoter approximately 500-2000Å; current carrier approximately 5-10 μ; and a layer of chromium of approximately 300-1000Å. Ball attach surface (still referring to FIGURE 11) may employ the first three layers of metalization of die attach surface or may employ all four layers. The first layer is adhesion promoter 14 which is preferably selected from among the same materials of that of promoter 6. Similar to that above, a current carrying layer 15, being preferably copper, is then deposited over promoter 14 and a third layer is metal 16 which preferably is nickel to provide a good surface for bonding of an AgCu eutectic alloy which is used to attach Balls 17 to the package; a gold protective layer may then be added. Thicknesses of the layers varies for the ball surface as follows: 500-2000Å; current carrier 3-5μ; buffer 2-5μ and gold 300-2000Å. Balls 17 may be Copper, but in most cases Balls 17 will be formed from a solder having a high melting point such as 95% Pb 5% Sn or 90% Pb 10% Sn. In this case metal 16 may be omitted and the balls attached directly to copper layer 15 for good bondability with balls 17, made of solder.

Capture pads 18 are placed upon both surfaces of the substrate 10 in electrical contact with vias 22. It should be noted that while individual vias are generally about 0.006 inch in diameter in the capture pads 18 provide a 0.010 inch diameter area in which to attach traces, balls, etc. which is much easier to work with. Capture pads 18 can be formed by preferably a photoresist-etch process, by physical masking, by a lift-off process, or by a copper thick film paste such as DuPont 9922 nitrogen fireable copper paste.

The die attach surface 11 further includes a die attach area 12 immediately surrounded by a multiplicity of wire bonding pads 19 for electrical attachment of the Die 30 through wire bonds 20 or flip chip attachment pads around the periphery or the underside of the die (not shown).

On BGA surface 13 of substrate 10 a heat spreader pad 21 is metallized using similar metalization options as described with respect to BGA surface 13.

Referring now to FIGURES 2 and 5 one embodiment of the package is illustrated which includes a passive insulative protection layer 31 to protectively cover the plurality of circuit traces 5 (see FIGURE 12) in the perimetrical area of substrate 10 which is not covered by lid 32. Layer 31 is preferably glass or epoxy or polyimide but may be any other adequately electrically insulative material.

Layer 31 does not necessarily extend completely over the entire substrate, rather it defines an opening in the center thereof large enough to expose the die 30 and wire bonding pads 19 or the flip chip contact pads. In order to bond a lid as described hereunder a seal ring 33 is provided atop layer 31 immediately perimetrically adjacent the geometrical shape defined by wire bonding pads 19. Seal ring 33 is generally constructed of the same material of which traces 5 are composed, which preferably is gold.

Lid 32 is preferably formed from nickel or Kovar and is normally deep drawn. It will be understood, however, that other methods are available and equally effective in forming lids. For some applications a gold plating is preferred on lid 32.

Attachment of lid 32 in the preferred embodiment of FIGURES 2 and 5 is by a conductive epoxy material, solder (Pb/Sn), AuGe brazing alloy material to bond the lid 32 in bonding zone 32a to the sealing ring 33. One of skill in the art will appreciate that other compounds are possible and that those listed are preferred.

In another embodiment of the invention the layer 31 is unnecessary due to the lid 34 covering the entire substrate 10. (See FIGURES 3 and 6). The seal ring 35, in this

case, is positioned along the outer perimeter of substrate 10 and outside of an area defined by the outermost row of vias 22. In other respects the lid 34 and zone 34a are as were lid 32 and bonding zone 32a.

A third embodiment, as illustrated in FIGURES 4 and 7, employs the passive insulating protective layer 31 in much the same manner as that in the embodiment of FIGURES 2 and 5. This embodiment differs in that instead of adhering a seal ring 33 and lid, a "blob" of epoxy material is placed atop the die and wire bonds thereby protecting them.

A further preferred embodiment is illustrated in FIGURE 13 in cross section wherein a ceramic lid 36 is employed which covers the entire package. The preferred materials for creating the lid 36 are the same as can be employed for the substrate, and the lid is preferably metalized on at least one if not both surfaces. The lid 36 is adhered to substrate 10 by an epoxy adhesive frame on bonding area 37.

The invention in each of the embodiments provides a high input/output (I/O) ratio to the overall size of the package without sacrificing clarity of signal or experiencing manufacturing difficulties (and concomitant cost).

While preferred embodiments have been shown and described, various modifications and substitutions may be made thereto without departing from the spirit and scope of the invention. Accordingly, it is to be understood that the present invention has been described by way of illustration and not limitation.

What is claimed is:

CLAIM 1. A Digital Integrated Circuit Package comprising:

a) a single layer substrate having a preselected pattern of vias;

b) a multiplicity of traces extending from a multiplicity of at least one of wire bonding pads and flip chip attachment pads to a multiplicity of vias to make electrical contact therebetween, said traces all being disposed upon said single layer substrate;

c) at least one protective structure disposed such that said vias, traces, wire bonding pads, at least one wire bond and at least one die are protected from environmental influence.

d) a multiplicity of electrically conductive balls disposed upon a second surface of said substrate said surface being opposed to a first surface of said substrate whereupon said at least one die is disposed.

CLAIM 2. A Digital Integrated Circuit Package as claimed in claim 1 wherein said single layer is of a fully sintered ceramic material.

CLAIM 3. A Digital Integrated Circuit Package as claimed in claim 2 wherein said ceramic material is an aluminum oxide (Al_2O_3)material.

CLAIM 4. A Digital Integrated Circuit Package as claimed in claim 2 wherein said ceramic is an aluminum nitride (AIN) material.

CLAIM 5. A Digital Integrated Circuit Package as claimed in claim 1 wherein said pattern of vias includes a closely patterned central section for thermal conduction and a peripheral pattern for signal/power.

CLAIM 6. A Digital Integrated Circuit Package as claimed in claim 5 wherein said signal/power vias maintain a columnar and row distance between each via of in the range of about 0.050 to 0.025 inch.

CLAIM 7. A Digital Integrated Circuit Package as claimed in claim 5 wherein said signal/power vias maintain a columnar and row distance between each via of about 0.050 inch and wherein column to column interstitial spacing is about 0.025 inch.

CLAIM 8. A Digital Integrated Circuit Package as claimed in claim 1 wherein said traces comprise a layered metalization including an adhesion promoter, current carrier, buffer, and protective layer.

CLAIM 9. A Digital Integrated Circuit Package as claimed in claim 8 wherein said traces are about 0.002 inch in width.

CLAIM 10. A Digital Integrated Circuit Package as claimed in claim 1 wherein said wire bonding pads comprise a layered metalization including an adhesion promoter, current carrier, buffer, and protective layer.

CLAIM 11. A Digital Integrated Circuit Package as claimed in claim 1 wherein said vias are filled with a bi-metallic composition.

CLAIM 12. A Digital Integrated Circuit Package as claimed in claim 11 wherein said bi-metallic composition is Copper-Tungsten.

CLAIM 13. A Digital Integrated Circuit Package as claimed in claim 1 wherein said vias are filled with a tri-metallic composition.

CLAIM 14. A Digital Integrated Circuit Package as claimed in claim 11 wherein said tri-metallic composition is Copper-Silver-Tungsten.

CLAIM 15. A Digital Integrated Circuit Package as claimed in claim 1 wherein said traces are spaced apart from one another by at least about 0.002 inch.

CLAIM 16. A Digital Integrated Circuit Package as claimed in claim 1 wherein said protective structure comprises a protective coating extending from a peripheral edge of said substrate into proximity with said wire bonding pads and a cover is bonded to said protective coating and extends over said wire bonding pads, wire bonds and at least one die.

CLAIM 17. A Digital Integrated Circuit Package as claimed in claim 1 wherein said protective structure comprises a cover bonded to an outer periphery of said substrate, said cover extending over the entirety of said package.

CLAIM 18. A Digital Integrated Circuit Package as claimed in claim 1 wherein said protective structure comprises a protective coating extending from an outer periphery of said substrate to within proximity of said wire bonding pads and wherein a "blob" of epoxy is applied to the package covering part of said protective coating and all of said wire bonding pads, wire bonds and at least one die.

CLAIM 19. A Digital Integrated Circuit Package as claimed in claim 16 wherein said cover is selected from the group consisting of metal and Kovar.

CLAIM 20. A Digital Integrated Circuit Package as claimed in claim 19 wherein said cover is plated with a conductive metal.

CLAIM 21. A Digital Integrated Circuit Package as claimed in claim 20 wherein said conductive metal is Gold.

CLAIM 22. A Digital Integrated Circuit Package as claimed in claim 17 wherein said cover comprises a ceramic material.

CLAIM 23. A Digital Integrated Circuit Package as claimed in claim 22 wherein said ceramic material is Al_2O_3.

CLAIM 24. A Digital Integrated Circuit Package as claimed in claim 22 wherein said ceramic material is AlN.

CLAIM 25. A Digital Integrated Circuit Package as claimed in claim 17 wherein said cover is selected from the group consisting of metal and Kovar.

CLAIM 26. A Digital Integrated Circuit Package as claimed in claim 25 wherein said cover is plated with a conductive metal.

CLAIM 27. A Digital Integrated Circuit Package as claimed in claim 26 wherein said conductive metal is Gold.

CLAIM 28. A Digital Integrated Circuit Package as claimed in claim 16 wherein said protective coating is glass.

CLAIM 29. A Digital Integrated Circuit Package as claimed in claim 16 wherein said protective coating is polyimide or epoxy.

CLAIM 30. A Digital Integrated Circuit Package as claimed in claim 16 wherein said protective coating is an insulative material.

CLAIM 31. A Digital Integrated Circuit Package as claimed in claim 18 wherein said protective coating is glass.

CLAIM 32. A Digital Integrated Circuit Package as claimed in claim 18 wherein said protective coating is polyimide.

CLAIM 33. A Digital Integrated Circuit Package as claimed in claim 18 wherein said protective coating is an insulative material.

CLAIM 34. A Digital Integrated Circuit Package as claimed in claim 1 wherein said first surface supports a series of metalizations including an adhesion promoter, a current carrier, a buffer and a protective finish.

CLAIM 35. A Digital Integrated Circuit Package as claimed in claim 34 wherein said promoter is selected from the group consisting of titanium, chromium, an alloy of titanium/tungsten and an alloy of titanium/molybdenum.

CLAIM 36. A Digital Integrated Circuit Package as claimed in claim 35 wherein said promoter is of a thickness of about 500 to about 2000 Angstroms.

CLAIM 37. A Digital Integrated Circuit Package as claimed in claim 34 wherein said current carrier is copper.

CLAIM 38. A Digital Integrated Circuit Package as claimed in claim 37 wherein said copper is in a thickness of about 5 to about 10 micrometers.

CLAIM 39. A Digital Integrated Circuit Package as claimed in claim 34 wherein said buffer is nickel.

CLAIM 40. A Digital Integrated Circuit Package as claimed in claim 39 wherein said nickel is in a thickness of about 1 to about 3.5 micrometers.

CLAIM 41. A Digital Integrated Circuit Package as claimed in claim 34 wherein said protective finish is gold.

CLAIM 42. A Digital Integrated Circuit Package as claimed in claim 41 wherein said gold is of a thickness of about 2 to about 3.5 micrometers..

CLAIM 43. A Digital Integrated Circuit Package as claimed in claim 1 wherein said second surface supports a series of metalizations including an adhesion promoter, current carrier and a protective layer.

CLAIM 44. A Digital Integrated Circuit Package as claimed in claim 43 wherein said adhesion promoter is selected from the group consisting of titanium, chromium, an alloy of titanium/tungsten and an alloy of titanium/molybdenum.

CLAIM 45. A Digital Integrated Circuit Package as claimed in claim 44 wherein said promoter is of a thickness of about 500 to about 2000 Angstroms.

CLAIM 46. A Digital Integrated Circuit Package as claimed in claim 43 wherein said current carrier is copper.

CLAIM 47. A Digital Integrated Circuit Package as claimed in claim 46 wherein said copper is in a thickness of about 3-5μ.

CLAIM 48. A Digital Integrated Circuit Package as claimed in claim 39 wherein said buffer is nickel.

CLAIM 49. A Digital Integrated Circuit Package as claimed in claim 48 wherein said nickel is in a thickness of about 2.0-5μ.

CLAIM 50. A Digital Integrated Circuit Package as claimed in claim 43 wherein said protective finish is gold.

CLAIM 51. A Digital Integrated Circuit Package as claimed in claim 50 wherein said gold is of a thickness of about 300-2000Å.

CLAIM 52. A Digital Integrated Circuit Package as claimed in claim 1 wherein said first surface supports a series of metalizations including an adhesion promoter, a current carrier, and a top metalization.

CLAIM 53. A Digital Integrated Circuit Package as claimed in claim 52 wherein said promoter is selected from the group consisting of titanium, chromium, an alloy of titanium/tungsten and an alloy of titanium/molybdenum.

CLAIM 54. A Digital Integrated Circuit Package as claimed in claim 53 wherein said promoter is of a thickness of about 500 to about 2000 Angstroms.

CLAIM 55. A Digital Integrated Circuit Package as claimed in claim 52 wherein said current carrier is copper.

CLAIM 56. A Digital Integrated Circuit Package as claimed in claim 55 wherein said copper is in a thickness of about 5 to about 10 micrometers.

CLAIM 57. A Digital Integrated Circuit Package as claimed in claim 52 wherein said top metalization is chromium.

CLAIM 58. A Digital Integrated Circuit Package as claimed in claim 57 wherein said chromium is of a thickness of about 300-1000Å.

CLAIM 59. A Digital Integrated Circuit Package substantially as hereinbefore described with reference to any one of Figures 2 to 13

The Patent Office

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Claims searched:	1-59	**Date of search:**	23 August 1996

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Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

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Int Cl (Ed.6): H01L 21/48, 23/498, 23/50; H05K 3/34

Other: Online:WPI

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
X,P	EP0664562 A1	AT&T (Fig 3, col 3 lines 18 to 21)	1 at least
X,P	US5490324 A	LSI Corp (Fig 4)	1
X	US5355283 A	Amkor Electronics, Inc. (whole document)	1 at least

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
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